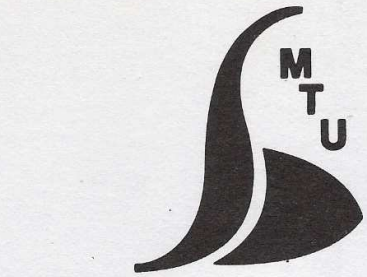

Micro
Technology
Unlimited

K-1016 16K BYTE MEMORY

6502 SYSTEM LOW POWER MEMORY

JANUARY 1, 1979

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K-1016 UNPACKING AND INSTALLATION

The K-1016 16K Memory is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Note that the board is shipped in a black conductive plastic bag. Since MOS integrated circuits are used, damage from static discharge is possible. It is helpful to reduce static by working in an area with concrete floors and a reasonable humidity level. If this is impossible, at least avoid wearing rubber soled shoes and move slowly in the work area. When unpacking or handling the board, touch the screw sticking up in the middle of the heatsink first and release it last. Note that the preceeding comments apply equally to the KIM-1 board which of course contains MOS IC's also.

Jumper socket S1 is shipped with jumpers installed for board addressing between 4000 and 7FFF. If at all possible, the board should be tested in the user's system with these jumpers intact. Following testing, they may be reconfigured as desired according to the table below:

ADDRESS RANGE	JUMPERS BETWEEN S1			ADDRESS RANGE	JUMPERS BETWEEN S1		
2000-5FFF	2-7	4-5		7000-AFFF	3-6	1-8	
3000-6FFF	2-7	1-8		8000-BFFF	3-6	1-8	4-5
4000-7FFF	2-7	1-8	4-5	9000-CFFF	3-6	2-7	
5000-8FFF	3-6			A000-DFFF	3-6	2-7	4-5
6000-9FFF	3-6	4-5		B000-EFFF	3-6	2-7	1-8

If desired, the user may install DIP a header wired with the jumpers or a standard 4 pole dipswitch into S1.

Connection to the KIM-1 should be as indicated in the accompanying chart. The easiest method of connection to the KIM is with an MTU model K-1005 motherboard/cardfile. Alternatively the user may obtain two 2x22 pin printed circuit board edge connectors (.156" contact spacing) such as the one supplied with the KIM and wire them together except for contact X. Wire length should not exceed 4 inches. Plug the KIM expansion connector into one of the sockets, make the indicated connections to the application connector, and make the indicated power connections. The 16K memory may then be plugged into the other connector.

Note that as shipped the board requires an unregulated voltage between +7 and +12 volts to operate the logic and another unregulated voltage between +14 and +20 volts to operate the memory chips such as provided by the expansion outputs of an MTU K-1000 power supply. The on-board regulators may be bypassed by shorting the two outside pins of each regulator IC together if the user wishes to use a regulated power source.

After connecting the KIM and the power supply, the system may be turned on. Pressing RESET on the KIM should initiate normal KIM operation. Set the address to 4000 and store different values there. Repeat at 5000, 6000, and 7000 so that each row of memory chips is tried. The KIM data display should be stable and reflect the data stored.

If all is well at this point the test program supplied with the K-1016 should be loaded through the KIM keyboard and dumped to cassette tape. The entry point is 0200. The test program generates a sequence of completely random bytes and stores them in memory in a scrambled order based on a random number. Following the store phase, the same pattern and order is regenerated and compared with memory contents. If comparison is successful, another test cycle with a different pattern and different store order is executed. Every 16 test cycles a 15 second delay is inserted between the store and verify phases to insure that memory refresh is working. The program should run indefinitely without stopping. If it does stop, locations 0000 and 0001 indicate the address of the failure and address 0002 shows the bit or bits in error.

At this point checkout of the K-1016 is complete and the user may now begin to use it for really big programs and lots of data.

SPECIFICATIONS

Access Time - Greater than 100NS data stable time prior to fall of system phase 2 clock
Cycle Time - Internally synchronized to 1 mHz system phase 2 clock.
Memory Type - 22 pin dynamic, high level clock (National MM5280)
Buffering - - Maximum of 1 LS TTL load on address and data bus
Power - - - - +7.5 volts unregulated 0.2 amp, +16 volts unregulated 75MA standby, 200MA maximum with 100% access.
Addressing - The 16K must be contiguous but may start at any 4K boundary. An 8-pin IC socket is provided for jumpers.
Adjustments - One, phase locked loop synchronization for timing generator
Sockets - - - The 32 memory IC's and address jumpers are socketed.
PC Board - - 11 inches wide 7.5 inches tall exclusive of gold plated edge connector, plated through holes.
Inclusions - Bare or assembled/tested board, instruction manual containing schematic, trouble-shooting tips, and memory diagnostic.

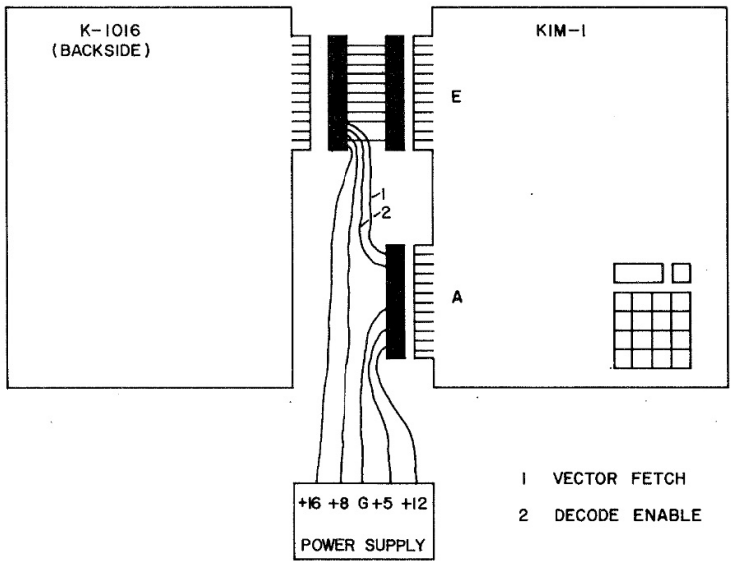
PIN CONNECTIONS

Signal	KIM	K-1016	Signal	KIM	K-1016
SYNC	E-1	N.C.	ADDR BUS 0	E-A	A
RDY	E-2	N.C.	ADDR BUS 1	E-B	B
PHASE 1	E-3	N.C.	ADDR BUS 2	E-C	C
IRQ	E-4	N.C.	ADDR BUS 3	E-D	D
SET OVERFLOW	E-5	N.C.	ADDR BUS 4	E-E	E
NON-MASK INT.	E-6	N.C.	ADDR BUS 5	E-F	F
RESET	E-7	N.C.	ADDR BUS 6	E-H	H
DATA BUS 7	E-8	8	ADDR BUS 7	E-J	J
DATA BUS 6	E-9	9	ADDR BUS 8	E-K	K
DATA BUS 5	E-10	10	ADDR BUS 9	E-L	L
DATA BUS 4	E-11	11	ADDR BUS 10	E-M	M
DATA BUS 3	E-12	12	ADDR BUS 11	E-N	N
DATA BUS 2	E-13	13	ADDR BUS 12	E-P	P
DATA BUS 1	E-14	14	ADDR BUS 13	E-R	R
DATA BUS 0	E-15	15	ADDR BUS 14	E-S	S
K6	E-16	N.C.	ADDR BUS 15	E-T	T
SING. STP. OUT	E-17	N.C.	PHASE 2	E-U	N.C.
+7.5 UNREG	N.C.	18	READ/WRITE	E-V	V
VECTOR FETCH	A-J	19	READ/WRITE	E-W	N.C.
DECODE ENAB.	A-K	20	*+16 UNREG*	***	X
+5 REG.	E-21	N.C.	PHASE 2	E-Y	Y
GROUND	E-22	22	RAM R/W	E-Z	N.C.

*** This signal must connect to the K-1016 only, not the KIM! ***

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

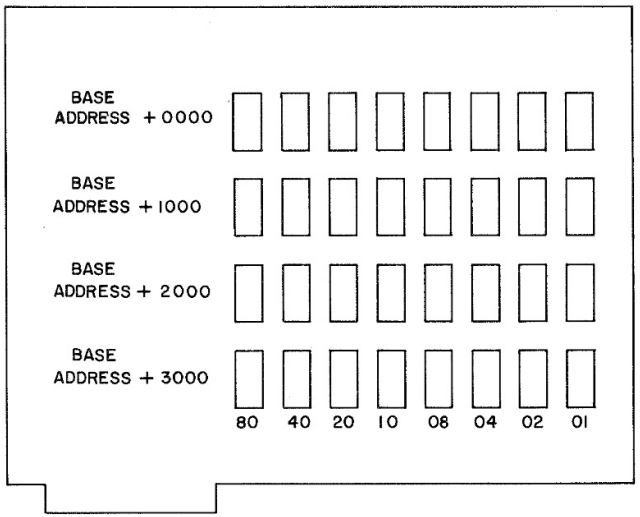
PARALLEL BUS
EXCEPT PIN X



1 VECTOR FETCH

2 DECODE ENABLE

MEMORY CHIP DATA BIT MAP

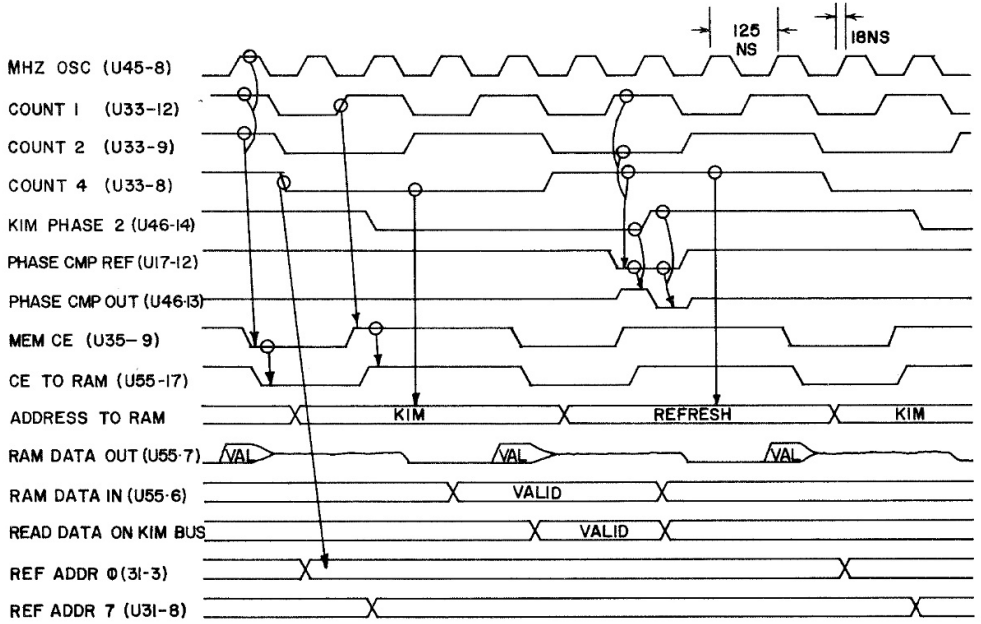


TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC. ± ANGLES ±		MICRO TECHNOLOGY UNLIMITED		
		K-1016 BIT MAP & CONNECTION		
APPROVALS	DATE			
DRAWN DBC	1-3-79			
CHECKED		SCALE	SIZE B	DRAWING NO.
		DO NOT SCALE DRAWING		SHEET 1-1

3

4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		MICRO TECHNOLOGY UNLIMITED		
APPROVALS	DATE	K-1016 MEMORY TIMING		
DRAWN DBC	12-78			
CHECKED		SCALE	SIZE B	DRAWING NO.
		DO NOT SCALE DRAWING		SHEET 1-1

PRINCIPLES OF OPERATION

The K-1016 16K dynamic memory uses several innovative design techniques to simultaneously achieve high reliability, totally transparent refresh, low power consumption, and complete KIM/VIM/AIM compatibility. Standard 22 pin 4K dynamic RAM's are utilized to provide the optimum combination of low cost, low power consumption, minimum support circuitry and multiple sources of supply. As stated above, refreshing is done in a manner that does not affect the operation of the 6502 processor at all. Therefore from the user's point of view, the board acts like a static memory board but with the cost and power advantages of dynamic boards.

The key to the board's remarkable properties is the 6502 bus itself. A symmetrical 1.0 mHz two-phase clock is used by the KIM-1. The 6502 microprocessor really accesses memory only during Phase 2 with Phase 1 being used for setup. Thus the K-1016 memory can use the 500NS period during Phase 1 to refresh the memory and then turn the memory over to the 6502 during phase 2. RAM chip access times approaching 300NS are required with this scheme but that figure is actually rather slow compared with modern 4K dynamic RAM standards. It is this "flip-flop" sharing between microprocessor and refresh that allows totally transparent refresh action under all operating conditions.

The memory array itself consists simply of 32 4K dynamic RAM chips of the 22 pin variety arranged in a 4 by 8 array. The primary reason for their use over other types of memory chips was cost and a long history of trouble-free reliable performance in large mainframe computers. Also they have the lowest average power consumption in this circuit of all available 4K RAM's. Although National Semiconductor MM5280's are used on factory assembled boards, many manufacturers produce compatible products. Exact details on the operation of 22 pin 4K dynamic RAM's may be found in the manufacturer's data sheets.

One signal required by the RAM chips is a clock signal that is 12 volts in amplitude. The leading edge of this signal causes the RAM's themselves to latch the state of the address inputs and hold it until clocked again. Data appears at the output after access time, which is typically 200NS, and remains until the clock returns to ground. When not clocked, the RAM's remain completely inactive, draw no power, and float their outputs. A power saver circuit generates a clock pulse only when a memory cycle is actually needed and only clocks the row of RAM's that was actually addressed. At all other times the memory array draws no power at all. If the KIM is not accessing the board, less than 17% of the possible memory cycles are active which rises to about 67% if the KIM is in a tight loop fetching and executing solely on the 16K board. An individual RAM chip will see from 1/4 to over 3/4 of this activity level depending on what the KIM is doing. The result is that the memory array runs from stone cold when the KIM is executing elsewhere to just cold when fully utilized.

All of the board's timing is derived from an 8mHz oscillator which is phase-locked to the rising edge of $\overline{\text{PHASE 2}}$ from the KIM. Each cycle of this oscillator represents a time slot for the timing generator which is 125 NS. U1 is the voltage controlled oscillator in the phase locked loop which is just a classic Schmidt trigger R-C oscillator. The 500 ohm pot determines the oscillator's free-running frequency and is set for a nominal frequency of 8.0mHz. This simple oscillator is made to act as a voltage controlled oscillator (VCO) by connecting a resistor (2.2K) to the R-C node. Changes in current through this resistor caused by voltage changes at its free end affect the oscillator's frequency. Although the linear VCO range is only 20% or so, this is ample for locking to the fixed crystal-controlled frequency of the KIM-1.

The phase detector is also rather unique. Since the phase angle of the lock between the on-board oscillator/counter chain and the KIM's $\overline{\text{PHASE 2}}$ clock affects the data transfer timing, it had to be controlled more tightly than a typical exclusive-or phase detector would provide. A tri-state buffer (U8) fills the bill. A 125NS pulse at a 1.0mHz rate from the first three stages of the counter

chain enables the tri-state buffer. The data input to the buffer is $\overline{\text{PHASE-2}}$ from the KIM. Ideal timing for data transfer between KIM and VM occurs when the trailing edge of $\overline{\text{PHASE 2}}$ occurs midway in the enable pulse. Under these conditions the output of the buffer floats for 7/8 of the cycle, is driven high for about 1/16 of the cycle, and then is driven low for the remaining 1/16 of the cycle before floating again. This wildly gyrating buffer output voltage is averaged by the low pass filter formed by R15 and C1. If $\overline{\text{PHASE 2}}$ turns off earlier in the enable window, the buffer output high time becomes less than the low time and the low-pass filter output voltage decreases thus speeding up the VCO which corrects for the error. The converse is true if $\overline{\text{PHASE 2}}$ becomes late. The exact equilibrium point can be changed by adjusting the 500 ohm pot, P1.

The 8mHz signal from the PLL next enters U12 which is a 4 bit binary counter. The first 2 stages function as a divide by 4 and time individual memory cycles which are actually 500NS long. The important output from the first two counter stages however is the MEM CE signal which controls the critical "chip enable" clock to the memory chips. As shown in the timing diagram, MEM CE is true for 5/2 of the 8mHz signal (313NS) and false for the other 3/2 (187NS). These times may vary slightly according to the 8mHz waveform symmetry but are far more stable than a single-shot timing generator would be.

The third stage of U12 awards even numbered memory cycles to the KIM and odd numbered ones to the refresh logic. This function is exercised via the signal SEL KIM ADDR. The last stage of U12 and a portion of U14 are set up to actually allow a refresh cycle on every fourth refresh oppertunity. This minimizes power consumption from excessive refreshing while allowing a complete memory refresh every millisecond. U13 is the gate that detects refresh cycles divisible by 4. U28 generates the 125NS enable pulse for the phase detector at the proper time with respect to the other signals.

The refresh address counter is 8 bits long and consists of U26. At the end of an actual refresh cycle, the counter increments by one in preparation for the next refresh cycle. In order to minimize noise, the 12 volt clock to the RAM chips is fully decoded thus only 8 RAM's are clocked on any one cycle. This decoding extends to refresh also simplifying the clock circuitry and preserving low noise during refresh cycles. Most other dynamic memory boards cannot afford the extra refresh time this technique costs but with a million opportunities for refresh every second on the K-1016, it is a very viable technique. The lower 6 bits of the refresh address counter address the 64 rows of the RAM's chips which must be refreshed. The remaining two bits address the four rows of RAM chips one at a time for refreshing.

A 8 bit 2 input address multiplexor is formed from U27 and U31. This multiplexor selects addresses from the refresh address counter when SEL KIM ADDR is false and selects addresses from the KIM when it is true. SEL KIM ADDR is roughly the inverse of KIM PHASE 2 but occurs about 50 to 100 NS earlier. U43 functions as a partial multiplexor for the remaining 4 RAM address bits by providing an unconditional high output when SEL KIM ADDR is false. The output of the address multiplexor drives the 12 address lines of the RAM array directly. Normally this would not be enough power to absorb the address line noise that occurs when the RAM's are clocked but since no more than 8 are clocked at once, they are quite adequate. U25 multiplexes three additional signals between the KIM and the refresh logic. Two of these are simply the two most significant address bits. The third is a signal that indicates whether a memory cycle is really needed. On the KIM side a cycle is only needed if the board is addressed. On the refresh side only every fourth cycle is needed.

U15 is the power saver and in conjunction with the level shifters/clock drivers determines which row of chips, if any, will be clocked during the current memory cycle. If MEM EN is not true during the cycle, then no RAM's are clocked during that cycle. Otherwise MEM CE is effectively inverted and routed to one of four level shifters according to address 12 and address 13 inputs to U15.

PRINCIPLES OF OPERATION

The clock driver circuit that accepts TTL levels from U15 and translates them to 12 volt levels is exceptionally simple, cheap, power conservative, and high in performance. Like the RAM array, the clock driver draws no power except when a clock pulse is being generated. Performance of the circuit when loaded by 8 RAM chips rivals that of $3 driver IC's with rise and fall times of less than 25NS. When the TTL level input goes positive, the NPN transistor saturates causing a low output level. The same edge creates a reverse voltage pulse through the 220PF capacitor which quickly turns the PNP off. When the TTL input goes negative the NPN turns off while a negative pulse of current through the 220PF capacitor turns the PNP on thus forcing the output to +12 volts. Since the load on the clock driver is purely capacitive, the PNP need not continuously pull the output up hard for the entire pulse width. The 100PF capacitor serves to speed up the NPN turnoff.

Looking now at the KIM side of the interface, U41 and U42 buffers the upper 8 KIM address bus bits and provides them in true form while part of U29 provides A13-A15 in complement form as well. These complement address bits in conjunction with a gate from U28 detects address references between 0000 and 1FFF and generates KIM DECODE ENABLE to allow the KIM monitor ROM's to function when A-K is disconnected from ground. An 8-input nand gate, U30, detects references between FF00 and FFFF and generates KIM VECTOR FETCH. A germanium diode in series with the gate output simulates the open-collector gate which is required.

The board address recognition circuitry is a bit strange to allow addressing the 16K memory on any 4K boundary. U40 is actually a 4 bit binary adder. This IC performs a 4 bit addition of its B inputs, which are the upper 4 bits of the KIM generated address, and its A inputs which are tied to 4 jumpers. The sum which appears at the outputs is the actual binary sum of the inputs. If overflow beyond 15 occurs, the sum output is modulo 16 of the real sum. The lower 2 bits of the sum select a row of RAM chips while the upper two bits activate BOARD ADRD only if they are both ones. Thus in order for the board to respond to an address, the sum of its upper 4 bits and the binary value of the jumpers must be between C and F (hexadecimal).

The KIM data bus is buffered both to and from the actual RAM array. Data from the bus passes through U52 and U54 on its way to the RAM DATA INPUT pins. The inversion of the data is cancelled by the data inversion inside the RAM itself. Data output from the RAM enters a tri-state latch which is necessary because data from the RAM's has disappeared by the time the KIM uses it. The latches have new data clocked into them at the end of every memory cycle but their contents are gated onto the KIM data bus only when the board is addressed and a write cycle is not being performed.

A portion of U13 generates the write enable signal to the RAM array. This signal is coincident with the RAM chip enable clock and is generated only when the board is addressed, a KIM cycle is being executed, and write enable is present on the KIM bus. Since only one row of RAM chips is actually clocked, the write enable signal can be distributed to all 32 RAM's in parallel.

Two 3-terminal regulators supply regulated +5 and +12 volts from unregulated input voltages. Minimal heatsinking is necessary due to the low power consumption of the board. The 1000uF filter capacitor on the +16 unregulated input allows the K-1000 power supply to power up to 48K of K-1016 memory as well as a KIM and K-1008 DAC all simultaneously. Typically a K-1008 Visible Memory can be thrown in also making for a really powerful system that runs on less than 25 watts of power. Negative 5 for the RAM chips is supplied by a charge pump and zener diode regulator. Two sections of U24 in parallel provide a 12 volt P-P signal at 1mHz which drives the network consisting of CR2, CR3, CR4, C3 and C4 which, without CR4, would produce about -11 volts. CR4 reduces this to -5 volts and in doing so limits the swing at U24-11 and 3 to about 6 volts P-P.

PARTS LIST FOR K-1016
16K MEMORY

DESCRIPTION	QUANTITY	DESIGNATION
74LS00	2	U8,47
74LS04	3	U1,3,18
74LS08	2	U6,7
74LS10	1	U17
74LS13	1	U45
74LS20	1	U34
74LS26	1	U29
74LS30	1	U19
74LS42	1	U36
74LS93	1	U33
74LS109	1	U35
74LS158	3	U20,30,32
74LS173	2	U2,4
74LS283	1	U5
74LS368	1	U46
74LS393	1	U31
MM5280 4K RAM CHIP	32	U9-16,21-28,37-44,48-55
1/4W 5% 270 OHM	1	R16
1/4W 5% 470 OHM	1	R19
1/4W 5% 1K	8	R5,6,8,10,11,12,14,15
1/4W 5% 2.2K	5	R7,9,13,17,18
1/4W 5% 10K	4	R1-4
TRIMPOT 500 OHM	1	P1
DIODE 1N270	1	CR1
DIODE 1N914	2	CR2,3
ZENER 5.1V 400MW	1	CR4
VOLT REG. LM340T-5	1	Q1
VOLT REG. LM342P-12	1	Q2
TRANSISTOR 2N3646	4	Q3,5,7,9
TRANSISTOR 2N4916	4	Q4,6,8,10
68PF 12V NP0 DISK	1	C88
100PF 12V X7R DISK	4	C17,33,69,85
220PF 12V X7R DISK	4	C16,32,68,84
.01UFD 12V Z5U DISK	2	C70,87
.047UFD 12V Z5U DISK	94	C1-4,6-15,19-31,35-67,72-83,89-108,110,111
.1UFD 12V Z5U DISK	4	C18,34,71,86
100UFD 16V ELEC	2	C5,109
1000UFD 25V ELEC	1	C0
8 PIN DIP SOCKET	1	S1
22 PIN DIP SOCKET	32	FOR MEMORY CHIPS
PC BOARD	1	PC1
HEATSINK	1	H1
SCREW,4-40X1/2 RH	1	MOUNT HEATSINK
NUT,HEX,4-40X.250	1	MOUNT HEATSINK
WASHER,FIBRE	2	UNDER HEATSINK

C110
C111
U50
U51
C109
C0
Q1
Q2
S1

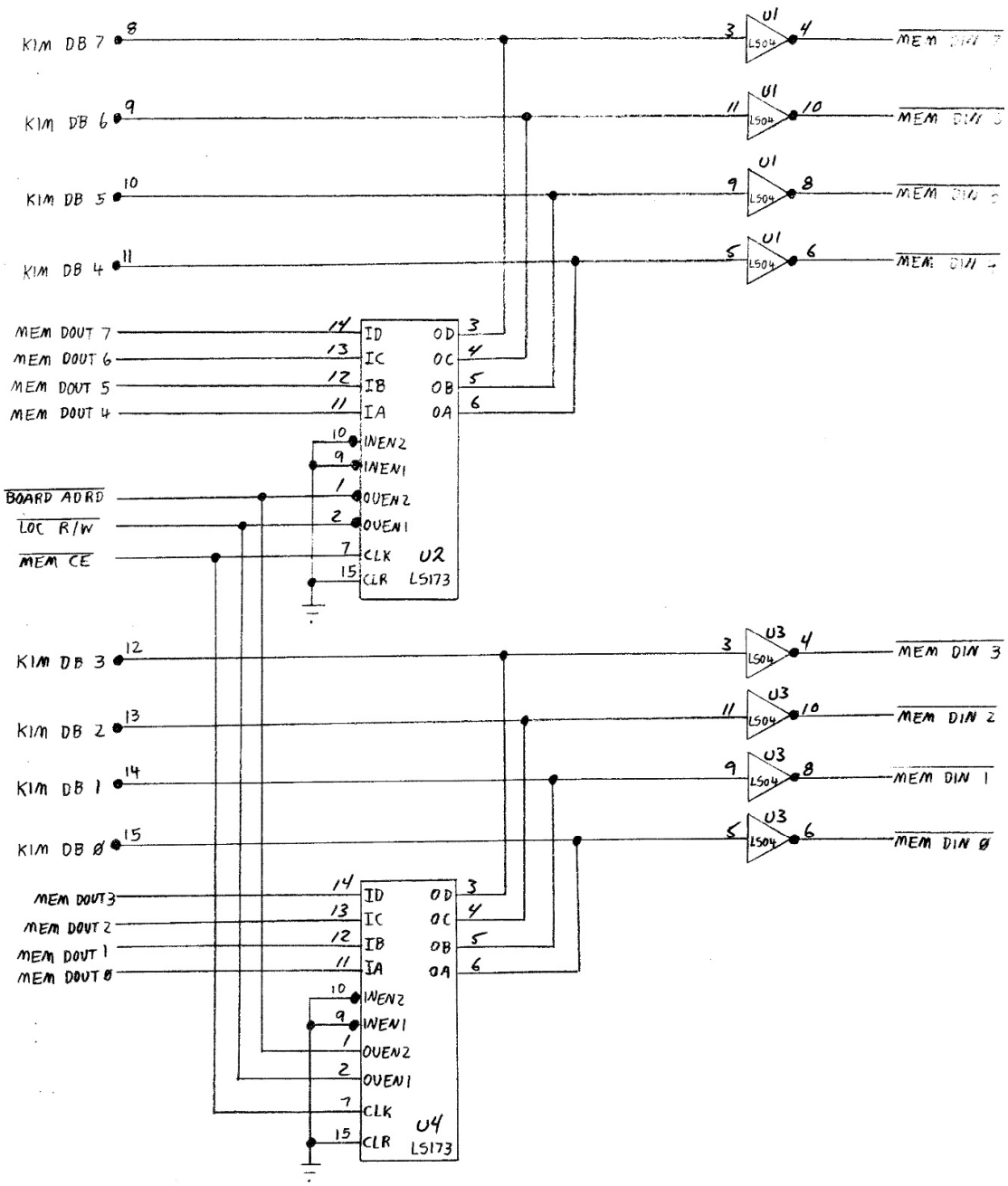
```
                        .PAGE  'EQUATES AND DATA STORAGE'
   3                ;       TEST AND EXERCISE PROGRAM FOR THE K-1016 16K MEMORY.
   4                ;           THE TEST IS A MEMORY FUNCTION TEST.  RANDOM BITS ARE STORED
   5                ;       IN A SCRAMBLED ORDER WHICH IS ALSO RANDOMLY DETERMINED.  AFTER
   6                ;       EVERY MEMORY LOCATION IS FILLED, THE SAME DATA AND SEQUENCE IS
   7                ;       REGENERATED AND MEMORY CONTENTS ARE CHECKED AGAINST IT.  THEN A
   8                ;       NEW SEQUENCE IS TRIED.  THIS IS ITERATED 16 TIMES WITH A 16
   9                ;       SECOND PAUSE BETWEEN THE WRITE AND VERIFY PHASE OF THE 16TH
  10                ;       ITERATION INSERTED TO VERIFY THE FUNCTIONALITY OF DYNAMIC RAM
  11                ;       REFRESH.  FOLLOWING THIS ANOTHER GROUP OF 16 ITERATIONS IS DONE
  12                ;           THIS PROGRAM IS SPECIFICALLY WRITTEN TO TEST 16K OF
  13                ;       CONTIGUOUS MEMORY. MODIFICATION TO TEST OTHER SIZES IS POSSIBLE
  14                ;       BUT THE AMOUNT TESTED MUST BE A POWER OF 2.
  15
  16
  17                ;       KIM SYSTEM EQUATES
  18
  19 1C22           KIMMON  =       X'1C22        ; ADDRESS OF SAVE MACHINE STATE ENTRY POINT
  20 4000           K16ORG  =       X'4000        ; ADDRESS OF 16K MEMORY
  21 4000           K16SIZ  =       16384         ; SIZE OF 16 MEMORY BOARD
  22 003F           K16SGB  =       K16SIZ-1/256  ; SIGNIFICANT UPPER ADDRESS BITS FOR 16K
  23
  24                ;       BASE PAGE DATA STORAGE
  25 0000                   .=      0
  26
  27                ;       MAIN PROGRAM DATA STORAGE
  28
  29 0000 0000      ERRADR: .WORD   0             ; ADDRESS OF DETECTED MEMORY ERROR
  30 0002 00        ERRBTS: .BYTE   0             ; ONES REPRESENT ERROR BITS
  31 0003 00        ITCNT:  .BYTE   0             ; ITERATION COUNT
  32
  33                ;       DATA STORAGE FOR RANDOM PATTERN TEST
  34
  35 0004 D204      RANDNO: .WORD   1234          ; RANDOM NUMBER REGISTER
  36 0006 0000      SEED:   .WORD   0             ; SAVES SEED FOR VERIFY
  37 0008 0000      ADDRCT: .WORD   0             ; DOUBLE BYTE ADDRESS COUNTER
  38 000A 0000      SCMEMA: .WORD   0             ; SCRAMBLED MEMORY ADDRESS AND ERROR ADDRES
  39
  40 000C                   .=      X'200         ; START PROGRAM CODE AT 200
  41
  42 0200 A9E0      MTEST:  LDA     #X'E0         ; INITIALIZE STACK POINTER
  43 0202 9A.               TXS
  44 0203 D8                CLD                   ; INSURE BINARY ARITHMETIC
  45
  46                ;       TEST: 16 PASSES WITH RANDOM DATA, PAUSE IN 16TH PASS
  47
  48 0204 A90F      MAIN10: LDA     #15           ; SET 16 ITERATION COUNT
  49 0206 8503              STA     ITCNT
  50 0208 209402    MAIN11: JSR     RAND          ; NEW PASS, GET A RANDOM
  51 020B A504              LDA     RANDNO        ; NUMBER IN RANDNO AND SAVE
  52 020D 8506              STA     SEED          ; AS SEED FOR VERIFY
  53 020F A505              LDA     RANDNO+1
  54 0211 8507              STA     SEED+1
  55 0213 204C02            JSR     RNDGEN        ; GENERATE A RANDOM DATA PATTERN IN 16K
  56 0216 A503              LDA     ITCNT         ; TEST IF LAST PASS
```

```
 57 0218 D011              BNE    MAIN15        ; SKIP OVER WAIT IF NOT
 58 021A A200              LDX    #0            ; WAIT FOR ABOUT 15 SECONDS IN A TIGHT LOOP
 59 021C A000      MAIN12: LDY    #0
 60 021E A921      MAIN13: LDA    #33
 61 0220 18        MAIN14: CLC
 62 0221 69FF              ADC    #-1
 63 0223 D0FB              BNE    MAIN14
 64 0225 88                DEY
 65 0226 D0F6              BNE    MAIN13
 66 0228 CA                DEX
 67 0229 D0F1              BNE    MAIN12
 68 022B A506      MAIN15: LDA    SEED          ; RESTORE RANDOM SEED FOR VERIFY PHASE
 69 022D 8504              STA    RANDNO
 70 022F A507              LDA    SEED+1
 71 0231 8505              STA    RANDNO+1
 72 0233 206902            JSR    RNDVER        ; VERIFY
 73 0236 D007              BNE    RNERLG        ; GO TO ERROR LOG IF ERROR
 74 0238 C603              DEC    ITCNT         ; DECREMENT AND CHECK ITERATION COUNT
 75 023A 10CC              BPL    MAIN11        ; LOOP UNTIL 16 ITERATIONS DONE
 76 023C 4C0402            JMP    MAIN10        ; REPEAT THE ENTIRE TEST WITH DIFFERENT
 77                                             ; DATA
 78
 79 023F 8502      RNERLG: STA    ERRBTS        ; STORE ERROR BITS
 80 0241 A50A              LDA    SCMEMA        ; STORE ERROR ADDRESS
 81 0243 8500              STA    ERRADR
 82 0245 A50B              LDA    SCMEMA+1
 83 0247 8501              STA    ERRADR+1
 84 0249 4C221C            JMP    KIMMON        ; GO TO KIM MONITOR
 85
 86                ;       RANDOM PATTERN STORED IN SCRAMBLED ORDER GENERATE ROUTINE
 87
 88 024C A900      RNDGEN: LDA    #0            ; INITIALIZE ADDRESS COUNTER
 89 024E 8508              STA    ADDRCT        ; TO 8192
 90 0250 A940              LDA    #K16SIZ/256
 91 0252 8509              STA    ADDRCT+1
 92 0254 209402    STORPH: JSR    RAND          ; GENERATE A RANDOM NUMBER
 93 0257 208202            JSR    MADDR         ; FORM A SCRAMBLED MEMORY ADDRESS
 94 025A A504              LDA    RANDNO        ; STORE A RANDOM BYTE
 95 025C A200              LDX    #0            ; INDIRECTLY THROUGH SCRAMBLED MEMORY
 96 025E 810A              STA    (SCMEMA,X)    ; ADDRESS AT SCMEMA
 97 0260 C608              DEC    ADDRCT        ; DECREMENT ADDRESS COUNTER
 98 0262 D0F0              BNE    STORPH        ; AND LOOP IF NOT ZERO
 99 0264 C609              DEC    ADDRCT+1
100 0266 D0EC              BNE    STORPH
101 0268 60                RTS                  ; RETURN WHEN DONE
102
103
104                ;       RANDOM PATTERN STORED IN SCRAMBLED ORDER VERIFY ROUTINE
105
106 0269 A940      RNDVER: LDA    #K16SIZ/256   ; INITIALIZE ADDRESS COUNTER
107 026B 8509              STA    ADDRCT+1
108 026D 209402    VERFPH: JSR    RAND          ; GENERATE A RANDOM NUMBER
109 0270 208202            JSR    MADDR         ; FORM SCRAMBLED MEMORY ADDRESS
110 0273 A10A              LDA    (SCMEMA,X)    ; GET DATA FROM MEMORY INDIRECTLY
111 0275 4504              EOR    RANDNO        ; THROUGH SCMEMA
```

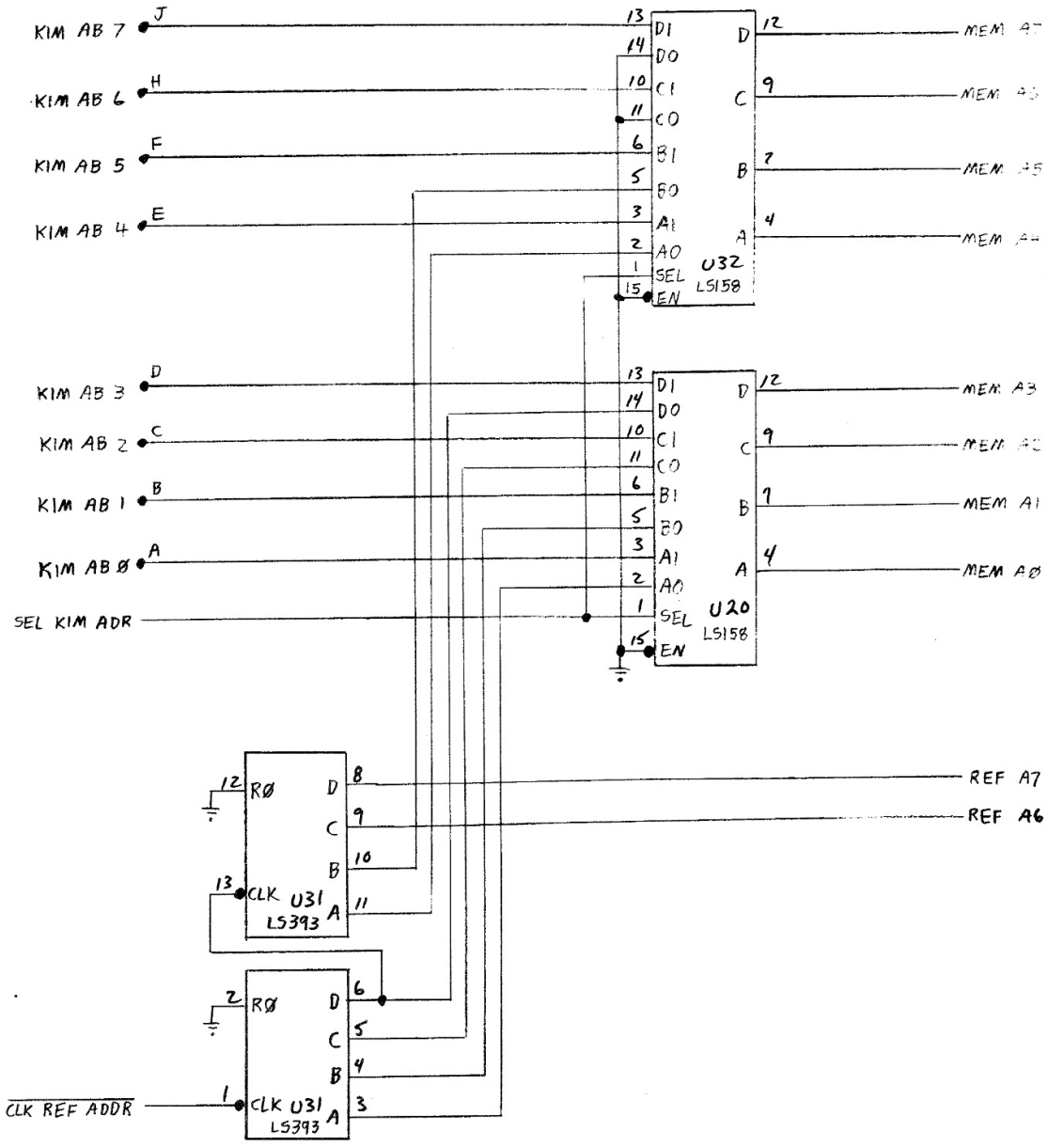
```
  112 0277 D008              BNE     VERRET          ; GO RETURN ON UNEQUAL COMPARE
  113 0279 C608              DEC     ADDRCT          ; DECREMENT ADDRESS COUNTER
  114 027B D0F0              BNE     VERFPH          ; AND LOOP IF NOT ZERO
  115 027D C609              DEC     ADDRCT+1
  116 027F D0EC              BNE     VERFPH
  117 0281 60       VERRET:  RTS                     ; RETURN
  118
  119               ;        SCRAMBLED MEMORY ADDRESS FORMATION ROUTINE
  120               ;        USES ADDRCT AND SEED TO FORM A SCRAMBLED ADDRESS IN SCMEMA
  121
  122 0282 A506     MADDR:   LDA     SEED            ; GET LOWER BYTE OF RANDOM NUMBER
  123 0284 4508              EOR     ADDRCT          ; EXCLUSIVE-OR WITH LOWER ADDRESS
  124 0286 850A              STA     SCMEMA          ; LOWER BYTE OF RESULT
  125 0288 A507              LDA     SEED+1          ; GET UPPER BYTE OF RANDOM NUMBER
  126 028A 4509              EOR     ADDRCT+1        ; EXCLUSIVE-OR WITH UPPER ADDRESS
  127 028C 293F              AND     #K16SGBT        ; SAVE SIGNIFICANT BITS OF RESULT
  128 028E 18                CLC
  129 028F 6940              ADC     #K16ORG/256     ; ADD IN FIRST PAGE NUMBER OF BOARD
  130 0291 850B              STA     SCMEMA+1        ; BEING TESTED
  131 0293 60                RTS                     ; RETURN
  132
  133
  134               ;        RANDOM NUMBER GENERATOR SUBROUTINE
  135               ;        ENTER WITH SEED IN RANDNO
  136               ;        EXIT WITH NEW RANDOM NUMBER IN RANDNO
  137               ;        USES 16 BIT FEEDBACK SHIFT REGISTER METHOD
  138               ;        DESTROYS REGISTER A AND Y
  139
  140 0294 A008     RAND:    LDY     #8              ; SET COUNTER FOR 8 RANDOM BITS
  141 0296 A504     RAND1:   LDA     RANDNO          ; EXCLUSIVE-OR BITS 3, 12, 14, AND 15
  142 0298 4A                LSRA                    ; OF SEED
  143 0299 4504              EOR     RANDNO
  144 029B 4A                LSRA
  145 029C 4A                LSRA
  146 029D 4504              EOR     RANDNO
  147 029F 4A                LSRA
  148 02A0 4505              EOR     RANDNO+1        ; RESULT IS IN BIT 3 OF A
  149 02A2 4A                LSRA                    ; SHIFT INTO CARRY
  150 02A3 4A                LSRA
  151 02A4 4A                LSRA
  152 02A5 4A                LSRA
  153 02A6 2605              ROL     RANDNO+1        ; SHIFT RANDNO LEFT ONE BRINGING IN CARRY
  154 02A8 2604              ROL     RANDNO
  155 02AA 88                DEY                     ; TEST IF 8 NEW RANDOM BITS COMPUTED
  156 02AB D0E9              BNE     RAND1           ; LOOP FOR MORE IF NOT
  157 02AD 60                RTS                     ; RETURN
  158
  159 0000                   .END
NO ERROR LINES
```

K-1016

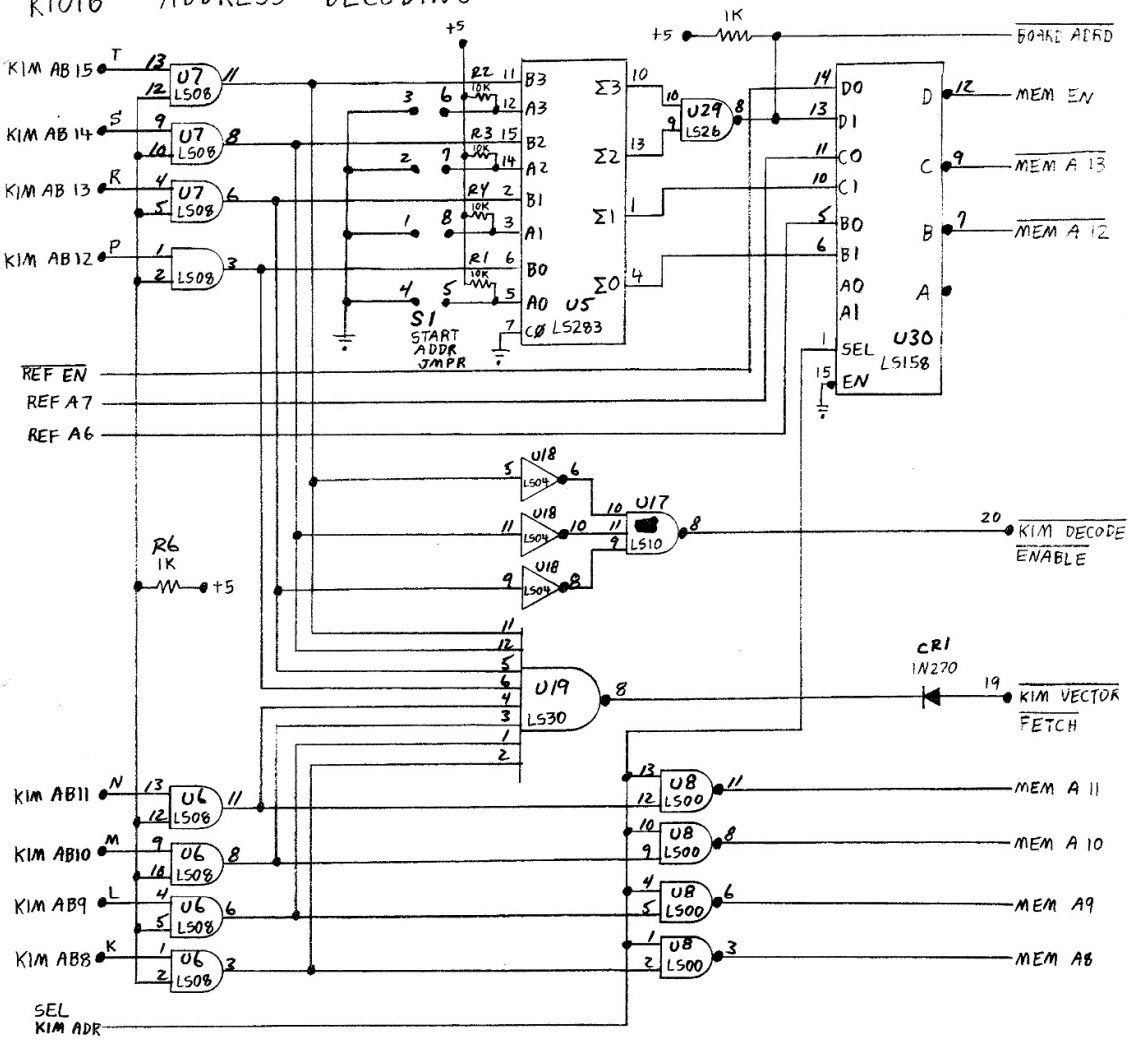
MEMORY DATA I/O



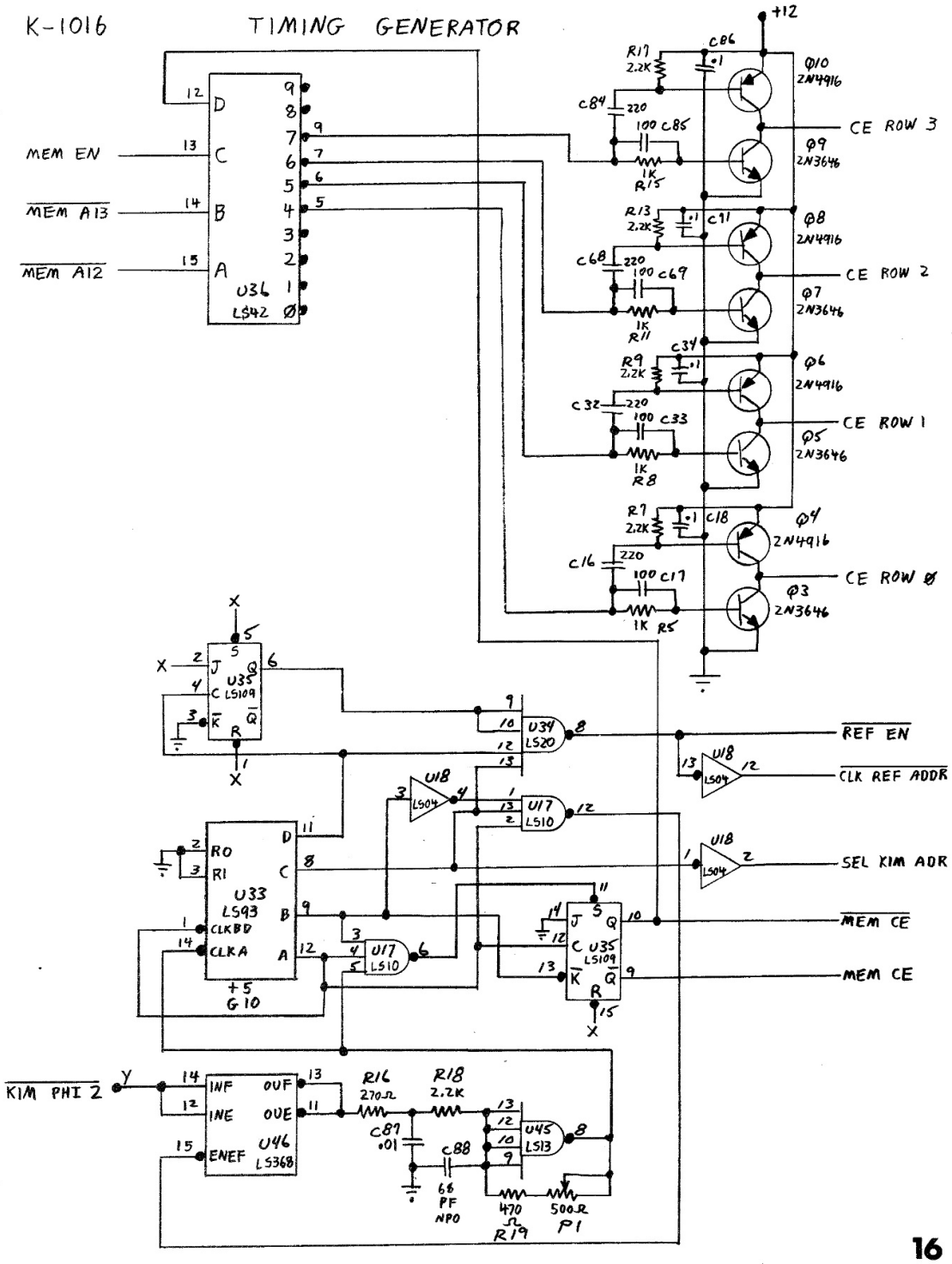
K-1016 REFRESH ADDRESS GENERATOR



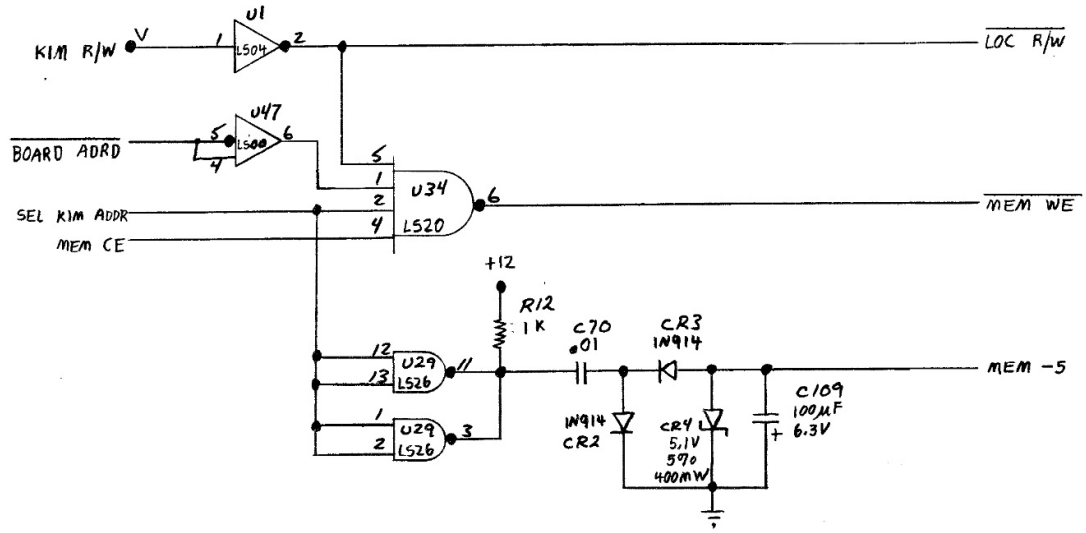
K1016 ADDRESS DECODING

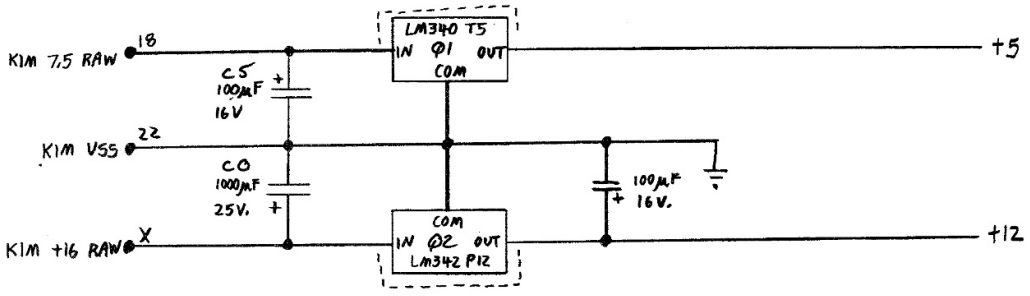


K-1016 TIMING GENERATOR

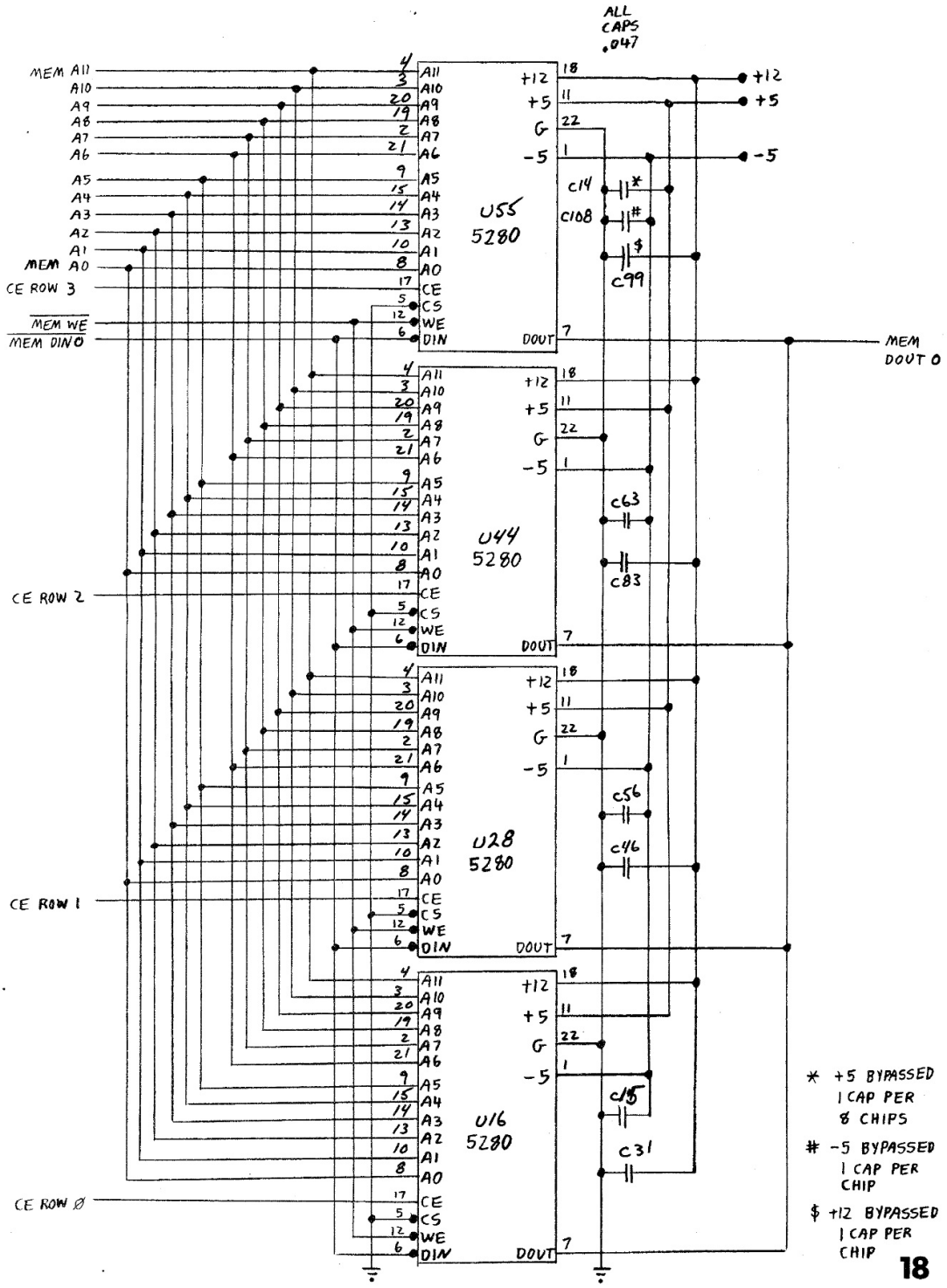


K-1016 MISCELLANEOUS

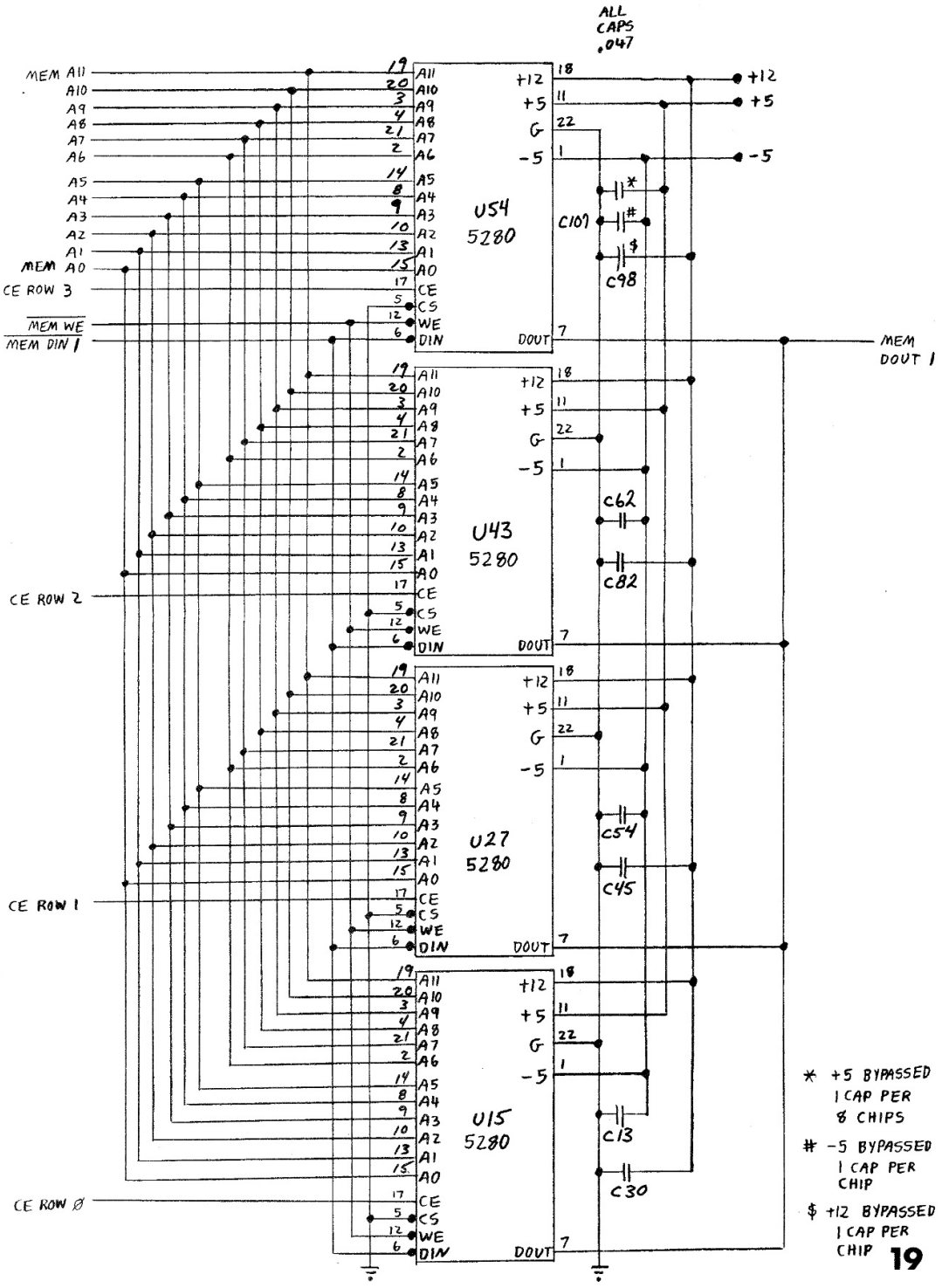




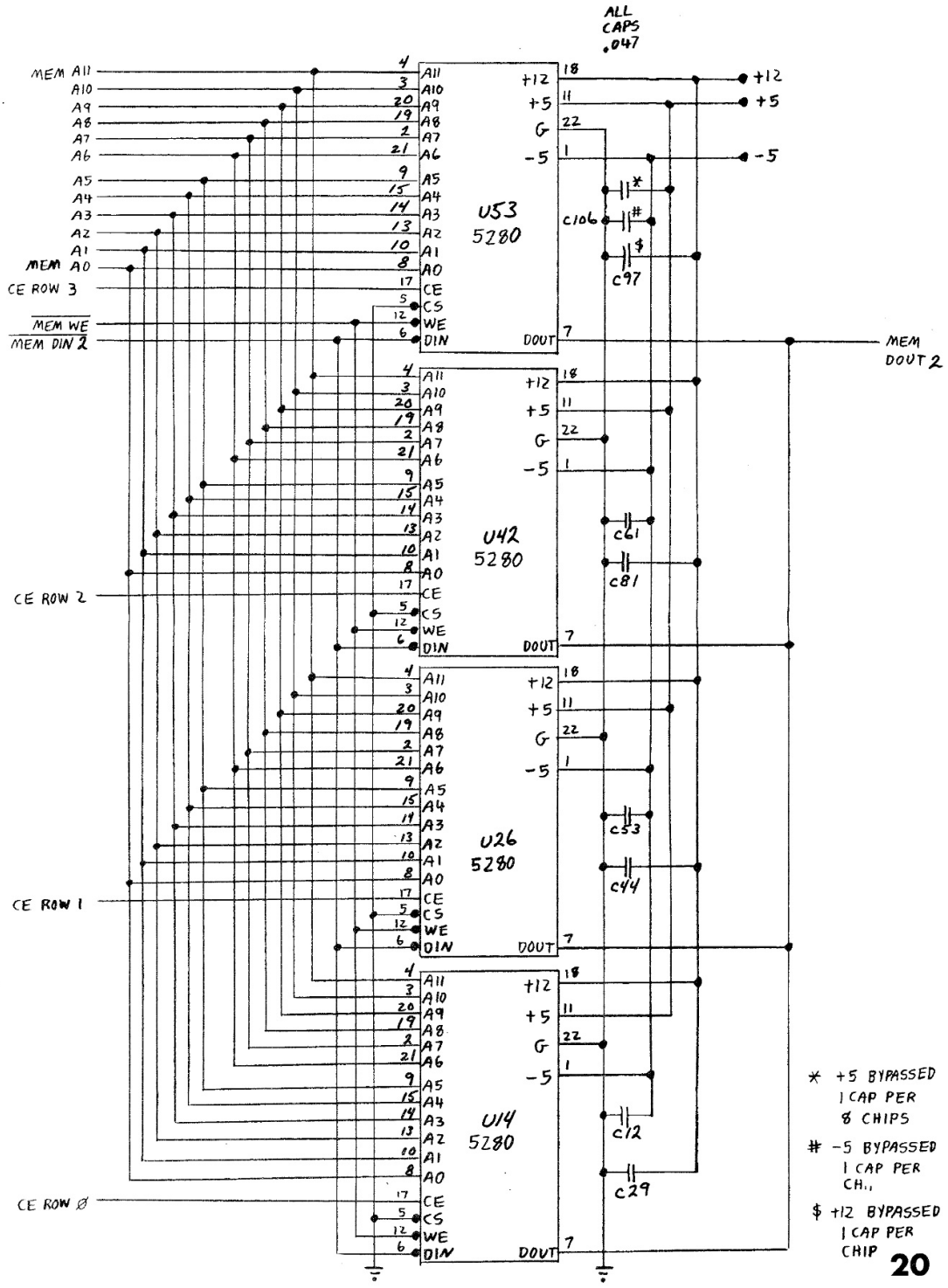
K-1016 RAM ARRAY BIT 0



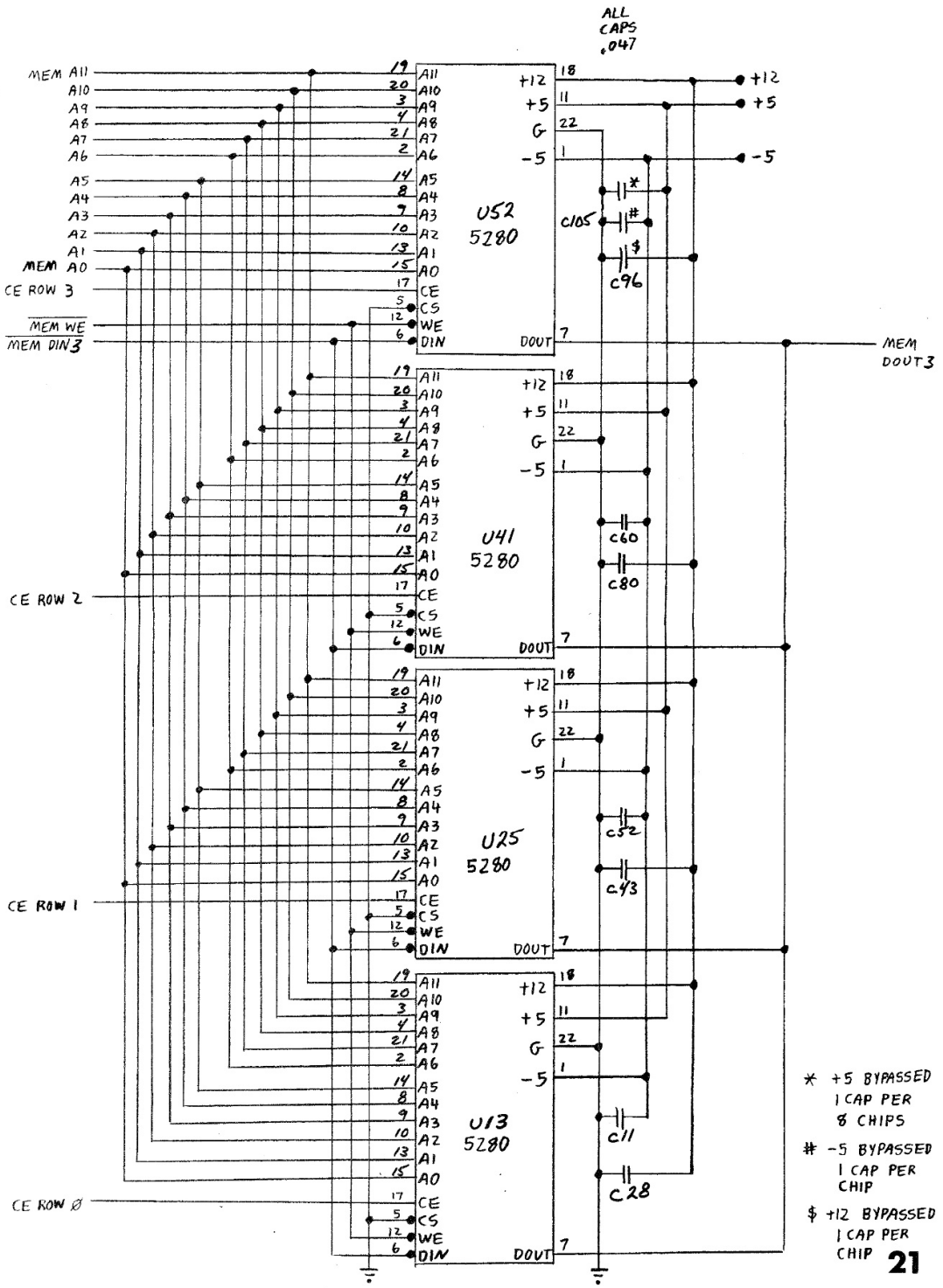
K-1016 RAM ARRAY BIT 1



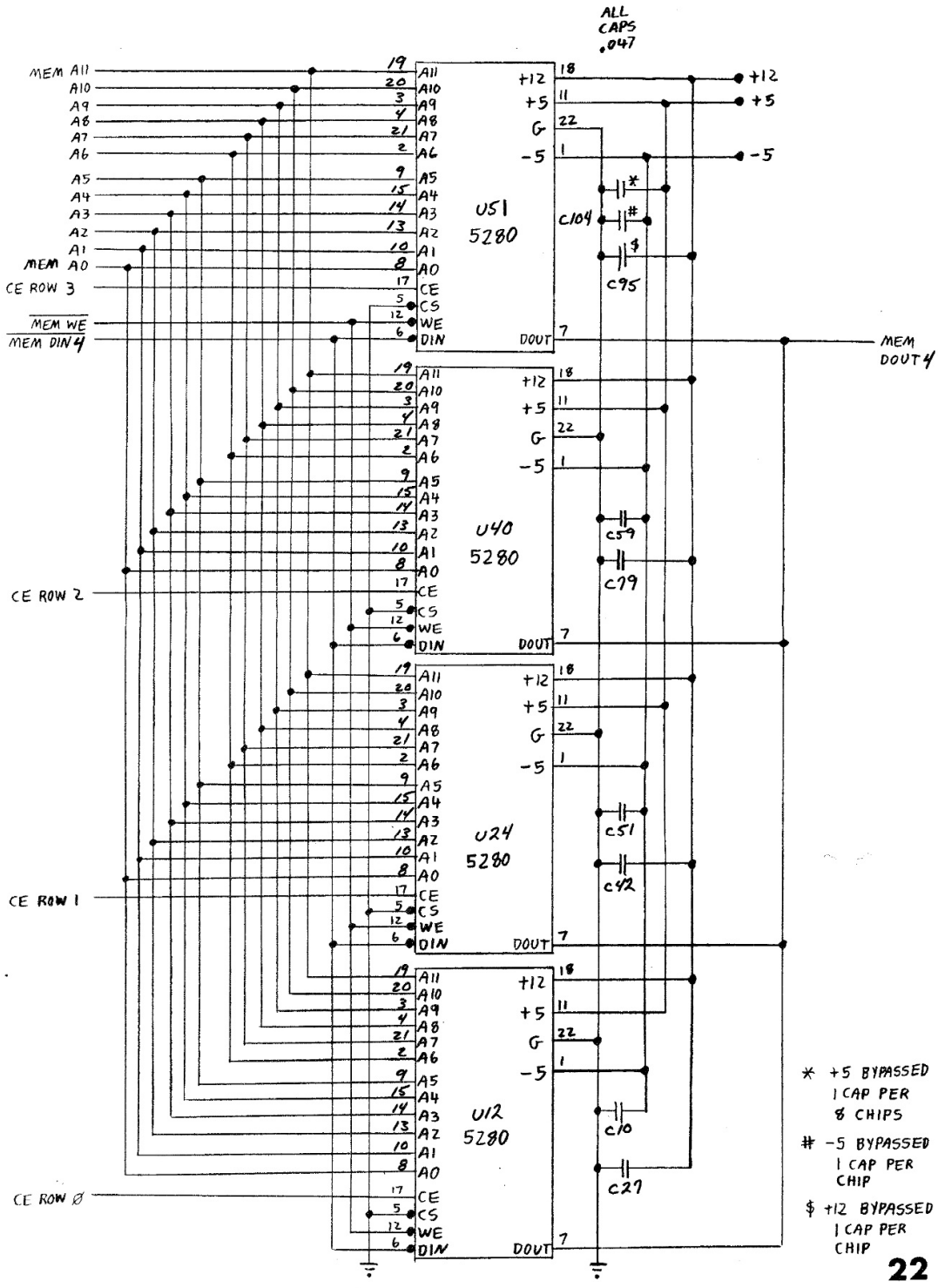
K-1016 RAM ARRAY BIT 2



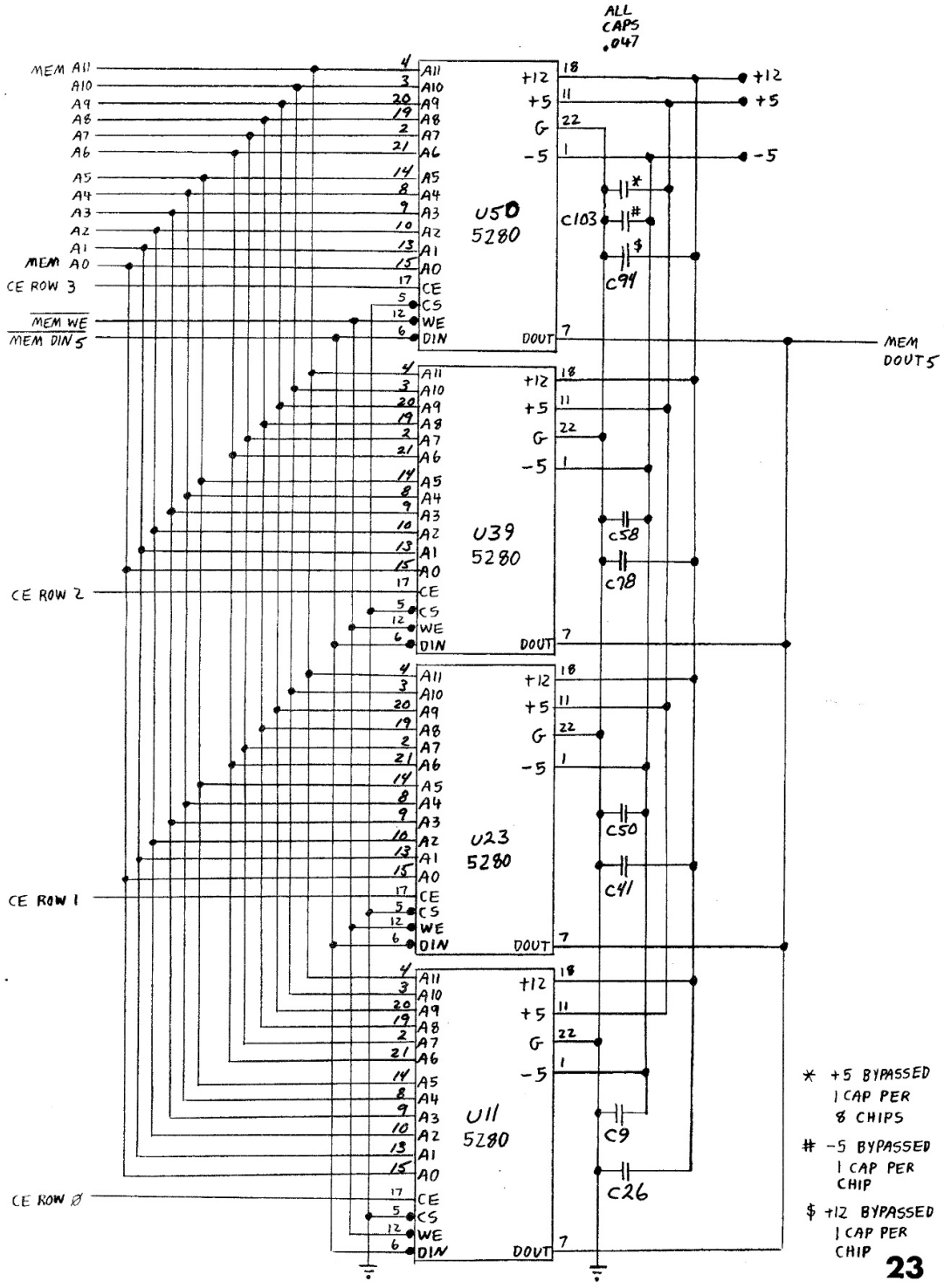
K-1016 RAM ARRAY BIT 3



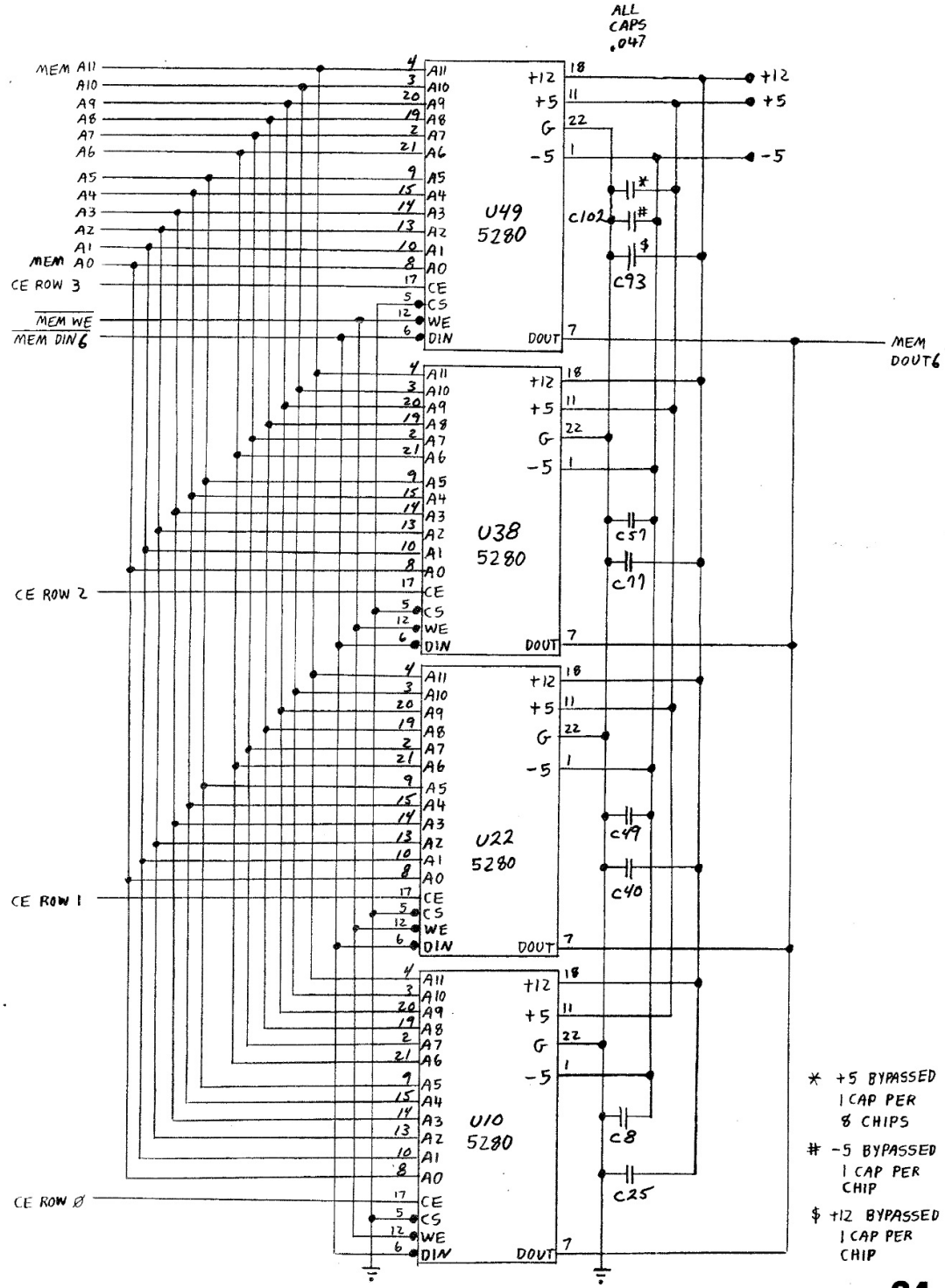
K-1016 RAM ARRAY BIT 4



K-1016 RAM ARRAY BITS



K-1016 RAM ARRAY BIT6



K-1016 RAM ARRAY BIT 7